

Customer No.: 31561  
Application No.: 10/709,606  
Docket NO.: 12239-US-PA

**AMENDMENT**

Please amend the application as indicated hereafter.

**In the Claims:**

Claim 1 (original): A DC level wandering cancellation circuit, comprising:

a low pass filter, for receiving an input voltage;

a high pass filter coupled to the low pass filter;

an amplifier coupled to the high pass filter for receiving a reference voltage and an output signal of the high pass filter;

a comparator coupled to the amplifier for receiving an output signal of the amplifier to compare the reference voltage with the output signal of the amplifier;

a resistor coupled between outputs of the high pass filter and the amplifier;

a control logic coupled to the comparator for receiving a compared result from the comparator; and

a switching means coupled between the high pass filter and the output of the amplifier, wherein the switching means is turned on for a predetermined interval by the control logic according to the compared result.

Claim 2 (original): The DC level wandering cancellation circuit of claim 1, wherein when the compared result from the comparator is from a high level to a low level, or from a low level to a high level, an output signal of the control logic changes to a high level to turn on the switching means.

Claim 3 (original): The DC level wandering cancellation circuit of claim 2, wherein the switching means is a transistor.

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Claim 4 (currently amended): The DC level wandering cancellation circuit of claim 1, wherein the low pass filter ~~further~~ comprises a first resistor and a first capacitor connected in parallel, and the high pass filter ~~further~~ comprises a second resistor and a second capacitor connected in series, wherein the second capacitor is coupled between the first and the second resistors.

Claim 5 (currently amended): The DC level wandering cancellation circuit of claim 4, wherein the switching means is coupled ~~between the control logic~~ a node between the comparator and the amplifier and a node between the second capacitor and the second resistor.

Claim 6 (original): The DC level wandering cancellation circuit of claim 1, wherein the control logic ~~further~~ comprises:

- a first inverter for receiving the compared result from the comparator;
- a second inverter coupled to an output terminal of the first inverter;
- a XOR gate configured to receive an output signal of the second inverter and the compared result from the comparator;
- a first NOR gate, having a first input terminal coupled to an output terminal of the XOR gate, and a second input terminal;
- a second NOR gate, having a first input terminal coupled to an output terminal of the first NOR gate, a second input terminal, and an output terminal coupled to the second input terminal of the first NOR gate;
- a first D-type flip flop, having an input terminal coupled to the output terminal of the second NOR gate, an output terminal, and a clock input terminal; and

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a second D-type flip flop, having an input terminal coupled to the output terminal of the first D-type flip flop, an output terminal coupled to the second input terminal of the second NOR gate, and a clock input terminal coupled to the clock input terminal of the first D-type flip flop for receiving a clock signal.

Claim 7 (currently amended): A DC level wandering cancellation method for a circuit having an inverting-gain amplifier, the method comprising:

receiving an input voltage using a low pass filter and a high pass filter, wherein the high pass filter is coupled to the low pass filter;

comparing an output signal of the inverting-gain amplifier with a reference voltage;  
and

feeding back the output signal of the inverting-gain amplifier to the inverting-gain amplifier when there is a state change in the compared result.

Claim 8 (original): The DC level wandering cancellation method of claim 7, wherein the state change is a level changed from high to low, or from low to high.